What is claimed is:

1. A semiconductor chip, comprising:

a surface protective film;

a bump projecting from the surface protective film for electrical connection between the semiconductor chip and another device; and

a surface interconnection provided on the surface protective film and having a smaller height than the bump.

2. A semiconductor chip as set forth in claim 1, which is to be bonded onto a surface of a solid body,

wherein the surface protective film covers a surface of the semiconductor chip which is opposed to the surface of the solid body,

wherein the bump serves for electrical connection to the solid body.

3. A semiconductor chip as set forth in claim 1, wherein the surface interconnection projects from the surface protective film.

4. A semiconductor chip as set forth in claim 1, wherein the surface interconnection is flush with the surface protective film.

5. A semiconductor chip as set forth in claim 1, wherein the surface interconnection is connected to the bump.

6. A semiconductor chip as set forth in claim 1,

wherein the bump includes a peripheral bump which is provided outside a device formation region of a semiconductor substrate which is a base body of the semiconductor chip.

7. A semiconductor chip as set forth in claim 6, wherein the peripheral bump is configured as surrounding the device formation region.

8. A semiconductor chip as set forth in claim 6, wherein the peripheral bump is provided in a scribe line region.

9. A semiconductor chip as set forth in claim 6, wherein the surface interconnection is connected to the peripheral bump.

10. A semiconductor chip as set forth in claim 6, wherein the peripheral bump is to be connected to a ground or a power source.

11. A production process for a semiconductor chip, comprising the steps of:

providing an internal interconnection on a semiconductor substrate;

forming a surface protective film over the internal interconnection;

forming an opening in the surface protective film to expose a portion of the internal interconnection;

forming a bump projecting from the surface

protective film on the portion of the internal interconnection exposed through the opening; and

forming a surface interconnection having a smaller height than the bump in a predetermined region on the surface protective film except a portion thereof formed with the opening.

12. A process as set forth in claim 11,

wherein the bump forming step includes the step of selectively depositing a conductive material on the portion of the internal interconnection exposed through the opening,

wherein the surface interconnection forming step includes the step of selectively depositing a conductive material in the predetermined region on the surface protective film except the portion thereof formed with the opening.

13. A process as set forth in claim 11,

wherein the conductive material is selectively deposited on the portion of the internal interconnection exposed through the opening and in the predetermined region on the surface protective film except the portion thereof formed with the opening, thereby to form a part of the bump and the surface interconnection,

wherein the conductive material is further selectively deposited on the part of the bump to complete

the bump which projects from the surface protective film.

14. A process as set forth in claim 11, further comprising the step of forming a recess in a region of the surface protective film on which the surface interconnection is to be formed before the formation of the bump and the surface interconnection, wherein the surface interconnection is formed in the recess.

15. A process as set forth in claim 14,

wherein the conductive material is selectively deposited in the opening and the recess to form a part of the bump and the surface interconnection,

wherein the conductive material is further selectively deposited on the part of the bump to complete the bump which projects from the surface protective film.

16. A process as set forth in claim 15, wherein the selective deposition of the conductive material in the opening and the recess includes the steps of:

forming a conductive material film over the surface protective film formed with the opening and the recess; and

removing the conductive material film except portions thereof formed in the opening and the recess.

17. A process as set forth in claim 16, wherein the removal of the conductive material film includes the step of partly polishing away the conductive material film

except the portions thereof formed in the opening and the recess for planarization thereof.

18. A process as set forth in claim 16, wherein the removal of the conductive material film includes the step of entirely polishing away the conductive material film except the portions thereof formed in the opening and the recess for planarization thereof.

19. A process as set forth in claim 14, wherein the recess has a bottom surface located at a lower level than a top surface of the internal interconnection.

20. A process as set forth in claim 14, further comprising the step of planarizing a surface of the surface protective film between the step of forming the surface protective film and the step of forming the opening and the recess.

21. A process as set forth in claim 11, wherein the bump includes a peripheral bump to be provided outside a device formation region of a semiconductor substrate which is a base body of the semiconductor chip.

22. A process as set forth in claim 21, wherein the peripheral bump is configured as surrounding the device formation region.

23. A process as set forth in claim 21, wherein the peripheral bump is formed in a scribe line region.

24. A process as set forth in claim 21, wherein the

surface interconnection is formed to be connected to the peripheral bump.